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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/680,054	10/05/2000	Shinji Nakamura	0819-430	7323

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EXAMINER

KEBEDE, BROOK

ART UNIT	PAPER NUMBER
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2823

DATE MAILED: 04/30/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

09/680,054

Applicant(s)

NAKAMURA ET AL.

Examiner

Brook Kebede

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 07 January 2002.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-60 is/are pending in the application.
- 4a) Of the above claim(s) 1-16 and 30-43 is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☐ Claim(s) 17-29 and 44-60 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☐ The proposed drawing correction filed on _____ is: a) ☐ approved b) ☐ disapproved by the Examiner.
- If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

- 13) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
- a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892) 4) ☐ Interview Summary (PTO-413) Paper No(s). _____
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948) 5) ☐ Notice of Informal Patent Application (PTO-152)
- 3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) 2,3. 6) ☐ Other: _____

DETAILED ACTION

Election/Restrictions

1. Applicants' election without traverse of Claims 17-29 and 44-60 in Paper No. 5 is acknowledged.
2. Claims 1-16 and 30-43 are withdrawn from further consideration pursuant to 37 CFR 1.142(b) as being drawn to a non-elected invention, there being no allowable generic or linking claim. Election was made **without** traverse in Paper No. 5.

Priority

3. Acknowledgment is made of applicants' claim for foreign priority based on an application filed in Japan on October 6, 1999. It is noted, however, that applicant has not filed a certified copy of the 11-285582 application as required by 35 U.S.C. 119(b).

Claim Rejections - 35 USC § 112

4. The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.
5. Claims 17-29, 47-51, 55, 57, and 59 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Although an attempt has been made to identify all instances of claim language non-compliance, such identification is extremely burdensome due to the large number of instances. Examples are provided herein below. Since such noncompliance confuses the claims to the extent that not all of the problems are readily apparent, then upon amendment, if an alternative

interpretation of claim language requires a change in the rejection, the new rejection may properly **made final**.

Claim 17 recites the limitation "a step of preparing a substrate in which surface is formed a depression having a closed figure when viewed from the substrate normal" in lines 3-5.

However, it is not clear how it is viewed from the substrate normal. Is it viewed by necked eye or by instrument or other viewing method? Since the scope of the claim can not be determined, the claim is vague and indefinite.

Claim 18 recites the limitation "a step of forming on a surface of said substrate a depression having a closed figure when viewed from the substrate normal" in lines 4-6.

However, it is not clear how it is viewed from the substrate normal. Is is viewed by necked eye or by instrument or other viewing method? Since the scope of the claim can not be determined, the claim is vague and indefinite.

Claim 20 recites the limitation "said major surface" in line 3. There is insufficient antecedent basis for this limitation in the claim.

Claim 45 recites the limitation "a step of applying onto said first semiconductor layer a resist pattern having an opening whose figure is either substantially an equilateral triangle, or substantially an equilateral hexagon when viewed from the substrate normal" in lines 3-6.

However, it is not clear how it is viewed from the substrate normal. Is it viewed by necked eye or by instrument or other viewing method? Since the scope of the claim can not be determined, the claim is vague and indefinite. Furthermore, it is not clear that how the resist pattern becomes either substantially an equilateral triangle, or substantially an equilateral hexagon. The claims lacks clarity in the scope and meaning.

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Claim 47 recites the limitation “a step of applying onto said first semiconductor layer a resist pattern whose figure is either substantially an equilateral triangle, or substantially an equilateral hexagon when viewed from the substrate normal” in lines 4-6. However, it is not clear how it is viewed from the substrate normal. Is it viewed by naked eye or by instrument or other viewing method? Since the scope of the claim can not be determined, the claim is vague and indefinite. Furthermore, it is not clear that how the resist pattern becomes either substantially an equilateral triangle, or substantially an equilateral hexagon. The claim lacks clarity in the scope and meaning.

Claim 49 recites the limitation “a step of forming a substrate having on a surface thereof a depression having a closed figure when viewed from the substrate normal” in lines 2-5. However, it is not clear how it is viewed from the substrate normal. Is it viewed by naked eye or by instrument or other viewing method? Since the scope of the claim can not be determined, the claim is vague and indefinite.

Claims 19-29, 50, 51, 55, 57 and 59 are rejected as being dependent of the rejected independent base claim.

Claim 48 is rejected as being dependent of claim 47.

Applicants' cooperation is requested in reviewing the claims structure to ensure proper claim construction and to correct any subsequently discovered instances of claim language noncompliance. See *Morton International Inc.*, 28USPQ2d 1190, 1195 (CAFC, 1993).

Claim Rejections - 35 USC § 102

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

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A person shall be entitled to a patent unless --

(a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

(e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) do not apply to the examination of this application as the application being examined was not (1) filed on or after November 29, 2000, or (2) voluntarily published under 35 U.S.C. 122(b). Therefore, this application is examined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

7. Claims 17-29 and 49-60 are rejected under 35 U.S.C. 102(e) as being anticipated by Kim et al. (US/6,337,223).

Re claim 17, Kim et al. disclose a method for the manufacture of a semiconductor device comprising: a step of preparing a substrate (i.e. sapphire substrate) (1) in which surface is formed a depression (i.e. GaN) (2) having a closed figure when viewed from the substrate normal; and a step of forming on said surface of said substrate a semiconductor layer having a hexagonal crystal structure (see Figs. 4A - 4D; Col. 4, line 1 - Col. 6, line 33).

Re claim 18, Kim et al. disclose a method for the manufacture of a semiconductor device comprising: a step of preparing a substrate (i.e. sapphire substrate) (1); a step of forming on a surface of said substrate a depression (i.e. GaN) (2) having a closed figure when viewed from the substrate normal; and a step of forming on said surface of said substrate a 5 semiconductor layer having a hexagonal crystal structure (see Figs. 4A - 4D; Col. 4, line 1 - Col. 6, line 33).

Re claim 19, as applied to claim 18 above, Kim et al. disclose all the claimed limitations including the limitation wherein said depression forming step is performed such that an inside face of said depression is defined by either a plane having a plane orientation of (1, -1, 0, 1) or its equivalent plane (see Figs. 4A – 4D; Col. 4, line 1 – Col. 6, line 33).

Re claim 20, as applied to claim 19 above, Kim et al. disclose all the claimed limitations including the limitation wherein said depression forming step is the step of forming on said major surface of said substrate defined by a (0, 0, 0, 1) plane a depression having a bottom face whose figure is either an equilateral triangle or an equilateral hexagon (see Figs. 4A – 4D; Col. 4, line 1 – Col. 6, line 33).

Re claim 21, as applied to claim 17 above, Kim et al. disclose all the claimed limitations including the limitation wherein said semiconductor layer forming step is the step of forming a semiconductor layer in which an inside face of said depression serves as a crystal growth surface (see Figs. 4A – 4D; Col. 4, line 1 – Col. 6, line 33).

Re claim 22, as applied to claim 21 above, Kim et al. disclose all the claimed limitations including the limitation wherein said semiconductor layer forming step includes a step in which said semiconductor layer crystal grows in a vertical direction from said inside face of said depression (see Figs. 4A – 4D; Col. 4, line 1 – Col. 6, line 33).

Re claim 23, as applied to claim 18 above, Kim et al. disclose all the claimed limitations including the limitation wherein said semiconductor layer forming step is the step of forming a semiconductor layer in which an inside face of said depression serves as a crystal growth surface (see Figs. 4A – 4D; Col. 4, line 1 – Col. 6, line 33).

Re claim 24, as applied to claim 23 above, Kim et al. disclose all the claimed limitations including the limitation wherein said semiconductor layer forming step includes a step in which

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said semiconductor layer crystal grows in a vertical direction from said inside face of said depression (see Figs. 4A – 4D; Col. 4, line 1 – Col. 6, line 33).

Re claim 25, as applied to claim 17 above, Kim et al. disclose all the claimed limitations including the limitation wherein said semiconductor layer forming step is the step of forming a layer which comprises Group III nitride-based compound semiconductor (see Figs. 4A – 4D; Col. 4, line 1 – Col. 6, line 33).

Re claim 26, as applied to claim 18 above, Kim et al. disclose all the claimed limitations including the limitation wherein said semiconductor layer forming step is the step of forming a layer which comprises Group III nitride-based compound semiconductor (see Figs. 4A – 4D; Col. 4, line 1 – Col. 6, line 33).

Re claim 27, as applied to claim 25 above, Kim et al. disclose all the claimed limitations including the limitation wherein said Group III nitride-based compound semiconductor layer is grown by a metal organic vapor epitaxy method (see Figs. 4A – 4D; Col. 4, line 1 – Col. 6, line 33).

Re claim 28, as applied to claim 26 above, Kim et al. disclose all the claimed limitations including the limitation wherein said Group III nitride-based compound semiconductor layer is grown by a metal organic vapor epitaxy method (see Figs. 4A – 4D; Col. 4, line 1 – Col. 6, line 33).

Re claim 29, as applied to claim 18 above, Kim et al. disclose all the claimed limitations including the limitation wherein said substrate preparing step is the step of preparing a sapphire substrate on which surface is formed a Group III nitride-based compound semiconductor layer; and wherein said depression forming step is the step of forming said depression in a surface of

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said Group III nitride-based compound semiconductor layer (see Figs. 4A – 4D; Col. 4, line 1 – Col. 6, line 33).

Re claim 49, Kim et al. disclose a method for the manufacture of a semiconductor substrate comprising: a step of forming a substrate having on a surface thereof a depression having a closed figure when viewed from the substrate normal; a step of forming on said surface of said substrate a semiconductor layer having a hexagonal crystal structure; and a step of taking out said semiconductor layer by removal of said substrate (see Figs. 4A – 4D; Col. 4, line 1 – Col. 6, line 33).

Re claim 50, as applied to claim 49 above, Kim et al. disclose all the claimed limitations including the limitation wherein said depression has an inside face defined by either a plane having a plane orientation of (1, -1, 0, 1) or its equivalent plane (see Figs. 4A – 4D; Col. 4, line 1 – Col. 6, line 33).

Re claim 51, as applied to claim 18 above, Kim et al. disclose all the claimed limitations including the limitation wherein said depression has, in said major surface of said substrate defined by a (0, 0, 0, 1) plane, a bottom face whose figure is either an equilateral triangle or an equilateral hexagon (see Figs. 4A – 4D; Col. 4, line 1 – Col. 6, line 33).

Re claim 52, Kim et al, disclose a method for the manufacture of a semiconductor substrate comprising: a step of forming a substrate having on a surface thereof a projection; a step of forming on said surface of said substrate a semiconductor layer having a hexagonal crystal structure; and a step of taking out said semiconductor layer by removal of said substrate (see Figs. 4A – 4D; Col. 4, line 1 – Col. 6, line 33).

Re claim 53, as applied to claim 52 above, Kim et al. disclose all the claimed limitations including the limitation wherein said projection has a side face defined by either a plane having a

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plane orientation of (1, -1, 0, 1) or its equivalent plane (see Figs. 4A – 4D; Col. 4, line 1 – Col. 6, line 33).

Re claim 54, as applied to claim 52 above, Kim et al. disclose all the claimed limitations including the limitation wherein said projection has, in said major surface of said substrate defined by a (0, 0, 0, 1) plane, a bottom face whose figure is either an equilateral triangle or an equilateral hexagon (see Figs. 4A – 4D; Col. 4, line 1 – Col. 6, line 33).

Re claim 55, as applied to claim 49 above, Kim et al. disclose all the claimed limitations including the limitation wherein said semiconductor layer forming step is the step of forming a layer of Group III nitride-based compound semiconductor (see Figs. 4A – 4D; Col. 4, line 1 – Col. 6, line 33).

Re claim 56, as applied to claim 52 above, Kim et al. disclose all the claimed limitations including the limitation wherein said semiconductor layer forming step is the step of forming a layer of Group III nitride-based compound semiconductor (see Figs. 4A – 4D; Col. 4, line 1 – Col. 6, line 33).

Re claim 57, as applied to claim 57 above, Kim et al. disclose all the claimed limitations including the limitation wherein said Group III nitride-based compound semiconductor layer is grown by hydride vapor phase epitaxy (see Figs. 4A – 4D; Col. 4, line 1 – Col. 6, line 33).

Re claim 58, as applied to claim 56 above, Kim et al. disclose all the claimed limitations including the limitation, wherein said Group III nitride-based compound semiconductor layer is grown by hydride vapor phase epitaxy (see Figs. 4A – 4D; Col. 4, line 1 – Col. 6, line 33).

Re claim 59, as applied to claim 49 above, Kim et al. disclose all the claimed limitations including the limitation said substrate forming step including: a step of preparing a sapphire substrate; and a step of forming on said sapphire substrate a Group III nitride-based compound

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semiconductor layer having said depression in a surface thereof (see Figs. 4A – 4D; Col. 4, line 1 – Col. 6, line 33).

Re claim 60, as applied to claim 52 above, Kim et al. disclose all the claimed limitations including the limitation said substrate forming step including: a step of preparing a sapphire substrate; and a step of forming on said sapphire substrate a Group III nitride-based compound semiconductor layer having said projection on a surface thereof (see Figs. 4A – 4D; Col. 4, line 1 – Col. 6, line 33).

8. Claims 44-60 are rejected under 35 U.S.C. 102(a) as being anticipated by Tomoika (JP/2002223417).

Re claim 44, Tomoika discloses a method for the manufacture of a semiconductor substrate including: a step of preparing a substrate (1) for crystal growth; a step of depositing on said crystal growth substrate a first semiconductor layer (2) having a hexagonal crystal structure; a step of exposing either a plane having a plane orientation of $(1, -1, 0, n)$ where said number n is an arbitrary number, or its equivalent plane by subjecting a part of said first semiconductor layer to an etching process; and after said exposing step, a step of depositing on said first semiconductor layer a second semiconductor layer having a hexagonal crystal structure (see Figs. 1-8 and Abstract).

Re claim 45, as applied to claim 44 above, Tomoika discloses all the limitations including a step of applying onto said first semiconductor layer a resist pattern having an opening whose figure is either substantially an equilateral triangle, or substantially an equilateral hexagon when viewed from the substrate normal; and a step of forming a depression by subjecting said first semiconductor layer to an etching process in which said resist pattern is used as a mask so that said depression has an inside face comprising either a plane having a plane orientation of $(1, -1,$

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0, n) where said number n is an arbitrary number, or its equivalent plane (see Figs. 1-8 and Abstract).

Re claim 46, as applied to claim 45 above, Tomoika discloses all the limitations including the limitation wherein said resist pattern has a plurality of said openings arrayed at equal intervals (see Figs. 1-8 and Abstract).

Re claim 47, as applied to claim 44 above, Tomoika discloses all the limitations including a step of applying onto said first semiconductor layer a resist pattern whose figure is either substantially an equilateral triangle, or substantially an equilateral hexagon when viewed from the substrate normal; and a step of forming a projection by subjecting said first semiconductor layer to an etching process in which said resist pattern is used as a mask so that said projection has a side face comprising either a plane having a plane orientation of (1, -1, 0, n) where said number n is an arbitrary number or its equivalent plane (see Figs. 1-8 and Abstract).

Re claim 48, as applied to claim 47 above, Tomoika discloses all the limitations including the limitation wherein said resist pattern comprises a plurality of said resist patterns arrayed at equal intervals (see Figs. 1-8 and Abstract).

Conclusion

9. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure Hayashi et al. (US/6,319,742), Nishikawa et al (US/6,323,053), Beaumont et al. (US/6,325,850), Kamiyama et al. (US/6,326,638), Tsuda et al. (US/6,335,546), Holland et al. (US/6,355,541), Funato et al. (US/6,362,016), Hiramatsu et al., Growth mechanism of GaN on sapphire with AlN buffer by MOVPE, *Journal of Crystal Growth*, 115, pp 628-633 (1991), and Yu et al., Study of the epitaxial-lateral-overgrowth (ELO) process for GaN on sapphire, *Journal of Crystal Growth*, 195 pp 333-339 (1998) also disclose similar inventive subject matter.

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Correspondence

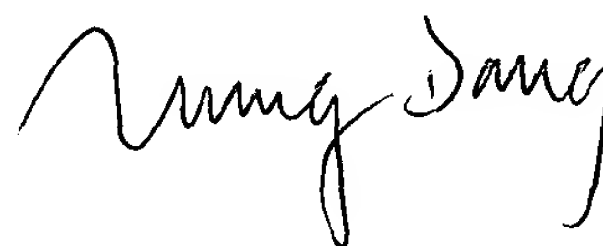
10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Brook Kebede whose telephone number is (703) 306-4511. The examiner can normally be reached on 8-5 Monday to Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael Fahmy can be reached on (703) 308-4918. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 308-7722 for regular communications and (703) 308-7722 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

Brook Kebede

BK
April 24, 2002



Trung Dang
Primary Examiner